

RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2016 Course : Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING

| Seat No: 3209 | P R No: 201007353 | Se | x: F | Nan | ne: | MAYEKAR MITHILI NARAYAN | |
|------------------|---------------------------------|-----------|------------------|-------------|-----|-------------------------|--|
| No Of Attempts : | 1. | | No Of Credits | Gra Obta | | SGPA | |
| ASIC Des | sign & FPGA | | | | | | |
| | | Theory | 4 | BB | P | | |
| | | IA | 2 | AB | P | | |
| Digital Sig | gnal Processors & Embedded | Systems | | | | | |
| | | Theory | 4 | BB | P | | |
| | | IA | 2 | CC | P | | |
| Design fo | r Testability & E-Waste Manage | gement | | | | | |
| | | Theory | 4 | BB | P | | |
| | | IA | 2 | CC | P | | |
| Processo | r Architecture & Parallel Proce | essing | | | | | |
| | | Theory | 4 | CC | P | | |
| | | IA | 2 | CC | P | | |
| Memory D | Design | | | | | | |
| | | Theory | 4 | CC | P | | |
| | | IA | 2 | AB | P | | |
| Parallel P | rocessing Lab | | | | | | |
| | | IA | 2 | BB | P | | |
| | | Practical | 2 | CC | P | | |
| FPGA & E | Embedded Systems Lab | | | | | | |
| | 1957/ | IA | 2 | BB | P | | |
| | | Practical | 2 | BB | Р | | |
| | | Total: | 38 | | | 6.26 P PASSES | |

| Grade | Grade Points | Performance |
|-------|-----------------|--------------|
| AO | 10 | Outstanding |
| AA | 9 | Excellent |
| AB | 8 | Very Good |
| BB | 7 | Good |
| ВС | 6 | Fair |
| CC | 5 | Satisfactory |
| FF | 0 | Fail |

Read By: pphle

Checked By : K

Date: 13 12 16

S.S.J. Figueiredo
Assistant Registrar-E(Proff.)

Leo V. Macedo Controller Of Examinations Prof. Y. V. Reddy Registrar

